IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/652,550
Priority Filing Date ..... August 31, 2000
Inventor ..... Keiji Jono et al.
Assignee ..... Micron Technology, Inc. and KMT Semiconductor, LTD
Priority Group Art Unit 2811
Priority Examiner ..... T. Tran
Attorney's Docket No. KM1-003
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents
Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.
(Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3817

Sir:

This is a preliminary amendment accompanying a Request for Divisional Application for the above-entitled patent application. Prior to examining the application, please enter the following amendments.

AMENDMENTS

In the Specification

At page 1, after the title, insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Divisional Application of U.S. Patent Application Serial No. 09/652,550, filed August 31, 2000, entitled "Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS," naming Keiji Jono, Hirokazu Ueda and Hiroyuki Watanabe as inventors.

In the Claims

Please cancel claims 1-32 without prejudice, amend claims 33, 34, 37, 42, 43, 46, 48, 50, 53, 55, 56 and 60 and add new claims 62-69 as noted below.

33. (Amended) A trench-isolated transistor comprising:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions, the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

34. (Amended) The trench-isolated transistor of claim 33, wherein at least some of the first sidewall forms a substantially straight linear segment.

35. The trench-isolated transistor of claim 33, wherein the second angle is between eighty and ninety degrees.

36. The trench-isolated transistor of claim 33, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

37. (Amended) The trench-isolated transistor of claim 33, wherein the first depth is between five and fifty percent of a total trench depth.

38. The trench-isolated transistor of claim 33, wherein the dielectric material filling the first and second isolation trench portions has a planar surface.

39. The trench-isolated transistor of claim 33, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

40. The trench-isolated transistor of claim 39, wherein the second angle is in a range of from eighty to ninety degrees.

41. The trench-isolated transistor of claim 33, wherein the transistor is formed as a part of a memory integrated circuit.

42. (Amended) A trench isolation structure formed in a semiconductor comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions.

43. (Amended) The trench isolation structure of claim 42, wherein at least some of the first isolation trench portion forms a substantially straight linear segment.

44. The trench isolation structure of claim 42, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

45. The trench isolation structure of claim 42, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

46. (Amended) The trench isolation structure of claim 42, wherein the first depth is between five and fifty percent of a total trench depth.

47. The trench isolation structure of claim 42, wherein the trench isolation structure is formed in a memory integrated circuit.

48. (Amended) A memory cell including:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region

being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side; the memory cell further including:

a bitline coupled to the drain; and

a wordline coupled to the gate.

49. The memory cell of claim 48, wherein the gate comprises polysilicon.

50. (Amended) The memory cell of claim 48, wherein at least some of the first sidewall forms a substantially straight linear segment.

51. The memory cell of claim 48, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

52. The memory cell of claim 48, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

53. (Amended) The memory cell of claim 48, wherein the first depth is between five and fifty percent of a total trench depth.

54. The memory cell of claim 48, wherein the memory cell is included within a DRAM integrated circuit.

55. (Amended) A DRAM comprising:

address decoding circuitry;

a group of bitlines coupled to the address decoding circuitry and extending in a first direction;

a group of wordlines coupled to the address decoding circuitry and extending in a second direction, each wordline in the group of wordlines intersecting each of the bitlines in the group of bitlines once at an intersection;

a plurality of memory cells each disposed at one of the intersections, each memory cell comprising:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second

sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

each memory cell further including:

one bitline of the group of bitlines coupled to the drain; and

one wordline of the group of wordlines coupled to the gate.

56. (Amended) The DRAM of claim 55, wherein at least some of the first sidewall forms a substantially straight linear segment.

57. The DRAM of claim 55, wherein the gate comprises polysilicon.

58. The DRAM of claim 55, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

59. The DRAM of claim 55, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

60. (Amended) The DRAM of claim 55, wherein the first depth is between five and fifty percent of a total trench depth.

61. The DRAM of claim 55, wherein the dielectric material filling the first and second isolation trench portions includes a planar outer surface.

New Claims

62. A memory cell including:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

an isolation trench disposed on a respective side of a portion of silicon, the isolation trench comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench; and

source and drain regions extending from the isolation trench across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

the memory cell further including:

a bitline coupled to the drain; and

a wordline coupled to the gate.

63. The memory cell of claim 62, wherein the gate comprises polysilicon.

64. The memory cell of claim 62, wherein at least some of the first sidewall forms a substantially straight linear segment.

65. The memory cell of claim 62, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

66. The memory cell of claim 62, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

67. The memory cell of claim 62, wherein the first depth is between five and fifty percent of a total trench depth.

68. The memory cell of claim 62, wherein the memory cell is included within a DRAM integrated circuit.

69. The memory cell of claim 62, wherein the isolation trench comprises a first isolation trench, the memory cell further comprising a second isolation trench, the first and second isolation trenches each disposed on a respective side of the portion of silicon, the second isolation trench comprising:

a third isolation trench portion having the first depth and having a third sidewall intersecting the surface at the first angle;

a fourth isolation trench portion within and extending below the third isolation trench portion, the fourth isolation trench portion having the second depth and including a fourth sidewall intersecting the third sidewall at the second angle; and wherein:

the dielectric material fills the first and second isolation trench portions;

the gate extends across the silicon portion from the first isolation trench to the second isolation trench; and

the source and drain regions extend between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

REMARKS

Claims 33, 34, 37, 42, 43, 46, 48, 50, 53, 55, 56 and 60 have been amended, claims 62-69 have been added and claims 1-32 have been canceled. Claims 33-69 are pending in the application. Examination of the pending claims is requested.

This application is a divisional application of U.S. Patent Application Serial No. 09/652,550 and is being filed responsive to a restriction requirement therein. Accordingly, claims 1-32 have been canceled without prejudice. Claims 33-69 remain in the application for consideration.

The amendments to claims 33, 34, 37, 42, 43, 46, 48, 50, 53, 55, 56 and 60 address minor informalities noted during review, however, these amendments do not alter the scope of the claims. No new matter is added by the amendments to claims 33, 34, 37, 42, 43, 46, 48, 50, 53, 55, 56 and 60.

New claims 62-69 are supported at least by text appearing at p. 6, line 18 through p. 14, line 5 of the application as originally filed. No new matter is added by new claims 62-69. New claims 62-69 distinguish over the art of record and are allowable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

This application is believed to be in condition for allowance and action to that end is requested. The Examiner is requested to telephone the undersigned in the event that the next office action is one other than a Notice

of Allowance. The undersigned is available during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Nov. 8, 2001

By: [signature]
Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

Version with markings to show changes made.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/652,550
Priority Filing Date ....August 31, 2000
Inventor ....Keiji Jono et al.
Assignee...............Micron Technology, Inc. and KMT Semiconductor, LTD
Priority Group Art Unit 2811
Priority Examiner .... T. Tran
Attorney's Docket No. KM1-003
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY PRELIMINARY AMENDMENT

Deletions are bracketed, additions are underlined.

In the Specification

At page 1, after the title insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Divisional Application of U.S. Patent Application Serial No. 09/652,550, filed August 31, 2000, entitled "Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS," naming Keiji Jono, Hirokazu Ueda and Hiroyuki Watanabe as inventors.

In the Claims

33. (Amended) A trench-isolated transistor comprising:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at [an] a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions, the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

34. (Amended) The trench-isolated transistor of claim 33, wherein at least some of the first [isolation trench portion comprises a] sidewall [at least some of which] forms a substantially straight linear segment.

37. (Amended) The trench-isolated transistor of claim 33, wherein the [first isolation trench portion has a] first depth [of] is between five and fifty percent of a total trench depth.

42. (Amended) A trench isolation structure formed in a semiconductor comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at [an] a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions.

43. (Amended) The trench isolation structure of claim 42, wherein at least some of the first isolation trench portion [comprises a sidewall at least some of which] forms a substantially straight linear segment.

46. (Amended) The trench isolation structure of claim 42, wherein the [first isolation trench portion has a] first depth [of] is between five and fifty percent of a total trench depth.

48. (Amended) A memory cell including:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at [an] a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain

region being disposed adjacent another side of the gate that is opposed to the one side;

the memory cell further including:

a bitline coupled to the drain; and

a wordline coupled to the gate.

50. (Amended) The memory cell of claim 48, wherein <u>at least some of</u> the first [isolation trench portion comprises a] sidewall [at least some of which] forms a substantially straight linear segment.

53. (Amended) The memory cell of claim 48, wherein the [first isolation trench portion has a] first depth [of] <u>is</u> between five and fifty percent of a total trench depth.

55. (Amended) A DRAM comprising:

address decoding circuitry;

a group of bitlines coupled to the address decoding circuitry and extending in a first direction;

a group of wordlines coupled to the address decoding circuitry and extending in a second direction, each wordline in the group of wordlines intersecting each of the bitlines in the group of bitlines once at an intersection;

a plurality of memory cells each disposed at one of the intersections, each memory cell comprising:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second

sidewall intersecting the first sidewall at [an] a second angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

each memory cell further including:

one bitline of the group of bitlines coupled to the drain; and

one wordline of the group of wordlines coupled to the gate.

56. (Amended) The DRAM of claim 55, wherein at least some of the first [isolation trench portion comprises a] sidewall [at least some of which] forms a substantially straight linear segment.

60. (Amended) The DRAM of claim 55, wherein the [first isolation trench portion has a] first depth [of] is between five and fifty percent of a total trench depth.

Claims 1-32 have been canceled and claims 62-69 have been added.

END OF DOCUMENT

EL844052799

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/652,550
Priority Filing Date ..... August 31, 2000
Inventor ..... Keiji Jono et al.
Assignee ..... Micron Technology, Inc. and KMT Semiconductor, LTD
Priority Group Art Unit 2811
Priority Examiner ..... T. Tran
Attorney's Docket No. KM1-003
TITLE: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS

Assistant Commissioner for Patents
Washington, D. C. 20231
Attention: Official Draftsman

SUBSTITUTE DRAWING REQUEST

Please enter the enclosed substitute formal drawings in the above-referenced application in place of drawings originally filed. The content of the drawings are identical to those now on file in this application.

Acknowledgment of receipt of the formal drawings and their acceptance into the file is requested.

Respectfully submitted,

Date: Nov 8 2001

By: _____

Frederick M. Fliegel, Ph.D.
Reg. No.: 36,138
WELLS, ST. JOHN, ROBERTS,
GREGORY & MATKIN P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828
(509) 624-4276

Enclosures: 3 Sheets of Formal Drawings, Figs. 1-6.